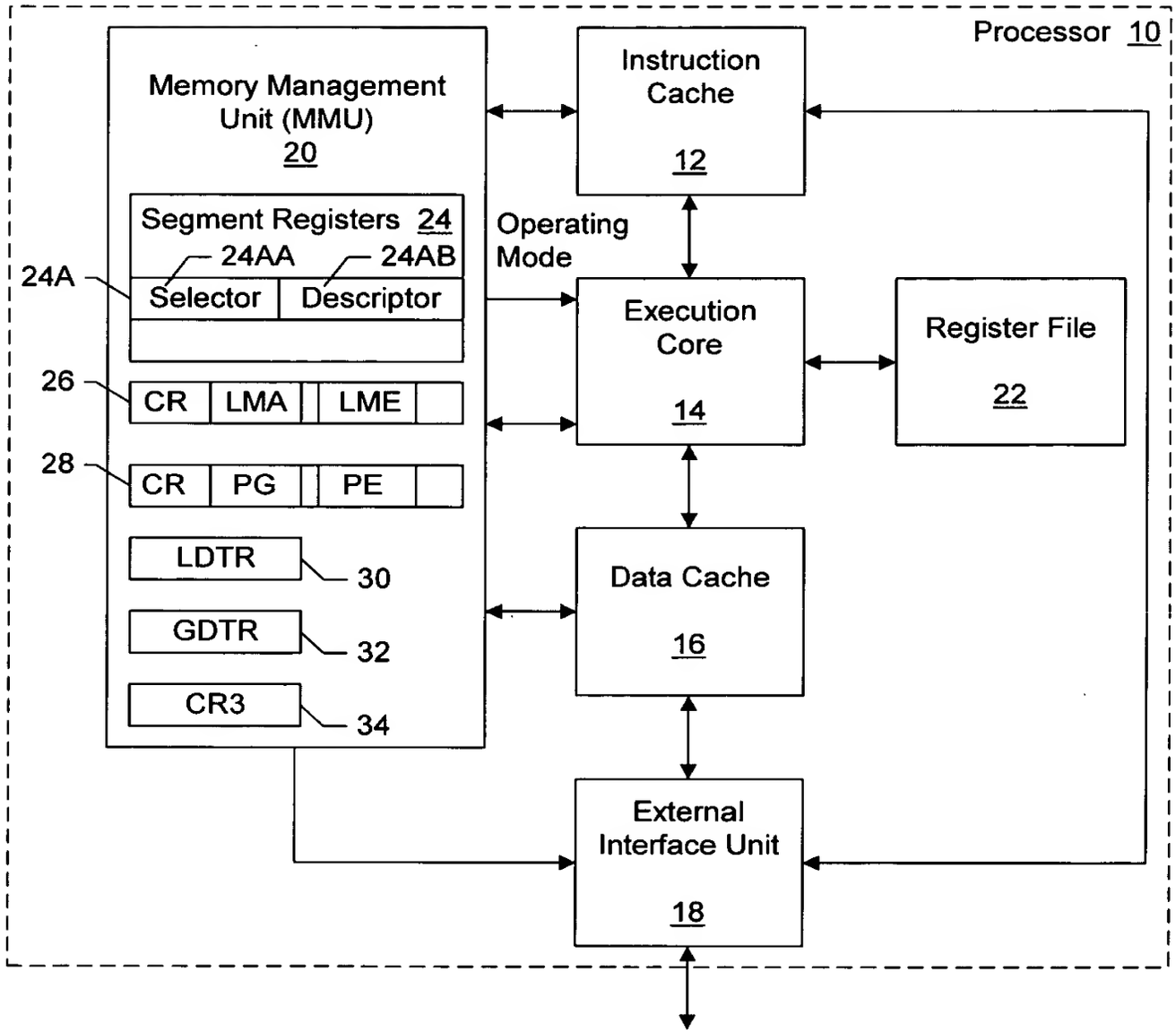
Processor 10
Memory Management Unit (MMU) 20
Segment Registers 24
24AA
24AB
24A
Selector
Descriptor
26
CR
LMA
LME
28
CR
PG
PE
LDTR
30
GDTR
32
CR3
34
Operating Mode
Instruction Cache 12
Execution Core 14
Register File 22
Data Cache 16
External Interface Unit 18

Fig. 1

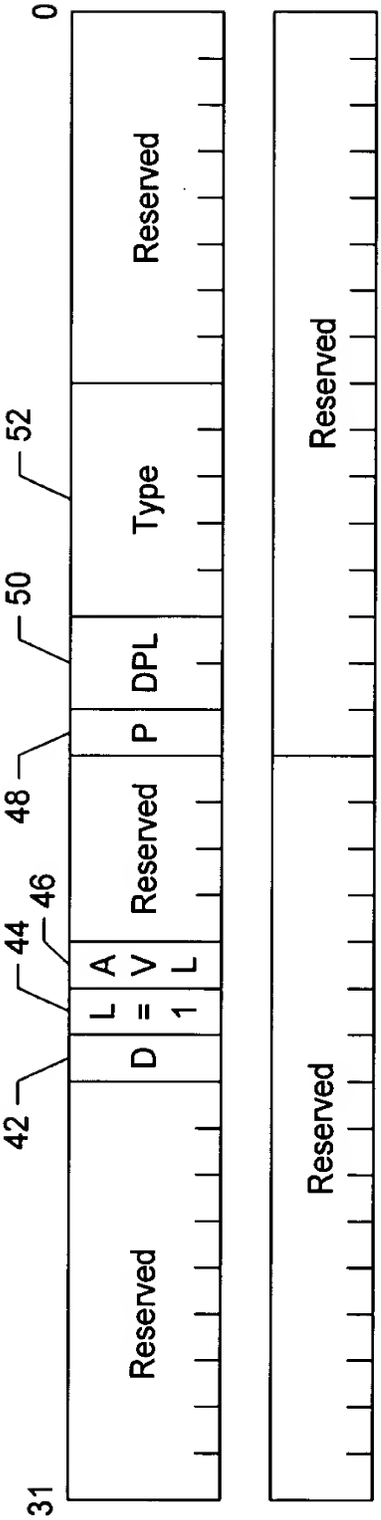
0
31
Reserved
D
L = 1
AVL
Reserved
P
DPL
Type
Reserved
Reserved
42
44
46
48
50
52
40

Fig. 2

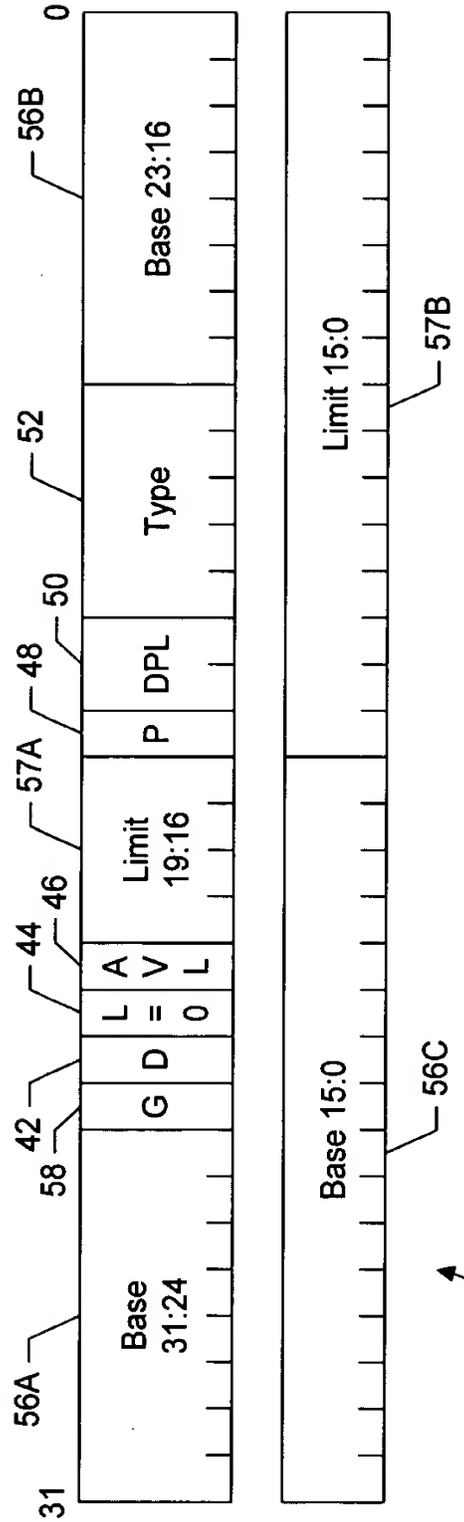
0
31
Base 31:24
G
D
L = 0
AVL
Limit 19:16
P
DPL
Type
Base 23:16
Base 15:0
Limit 15:0
42
44
46
48
50
52
56A
56B
56C
57A
57B
58
54

Fig. 3

LMA	CS L Bit	CS D Bit	Operating Mode
0	x	0	16 Bit Mode
0	x	1	32 Bit Mode
1	0	0	16 Bit Compatibility Mode
1	0	1	32 Bit Compatibility Mode
1	1	0	32/64 Mode
1	1	1	Reserved

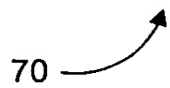

Fig. 4

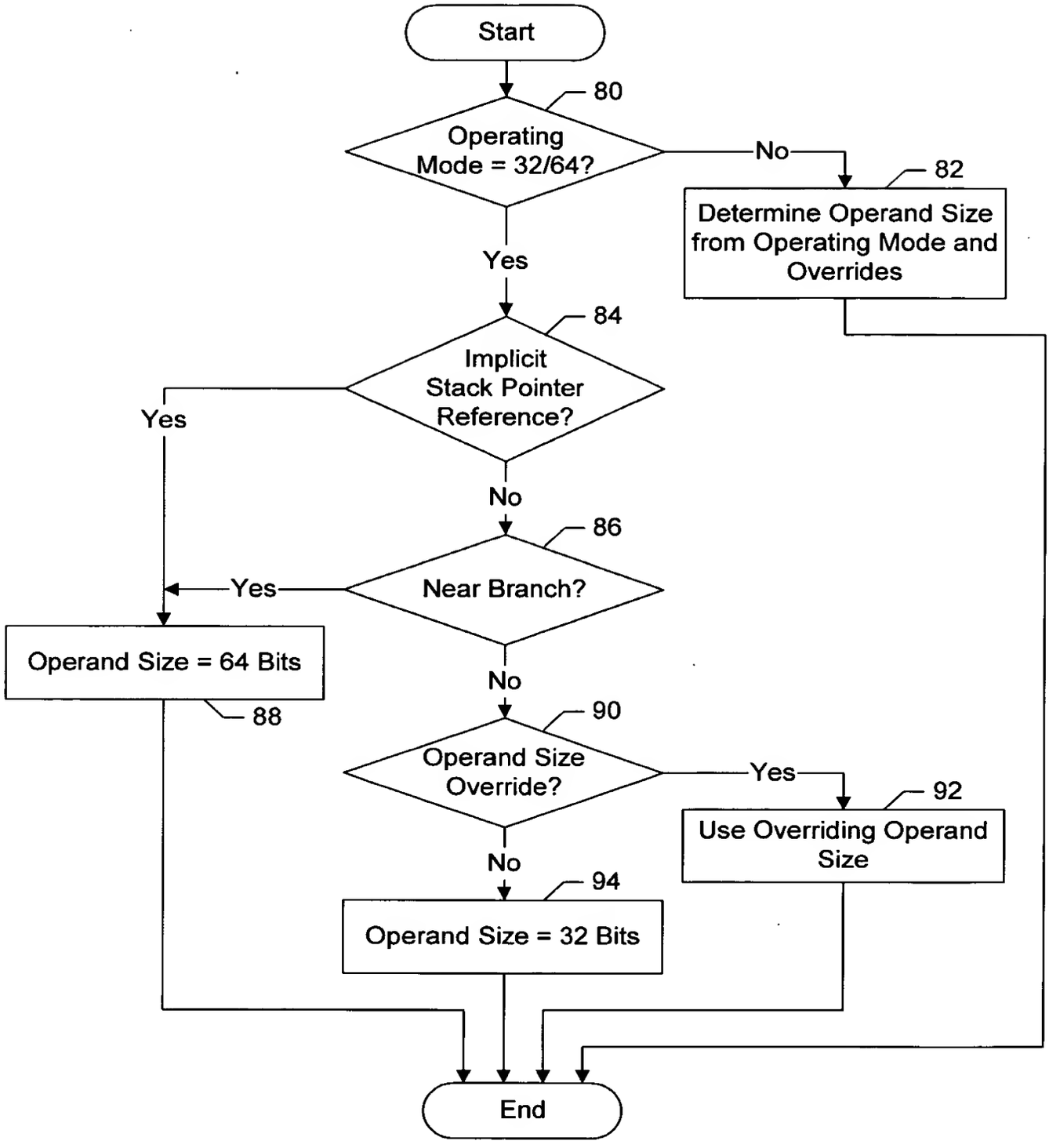
Start
80
Operating Mode = 32/64?
No
82
Determine Operand Size from Operating Mode and Overrides
Yes
84
Implicit Stack Pointer Reference?
Yes
No
86
Near Branch?
Yes
Operand Size = 64 Bits
88
No
90
Operand Size Override?
Yes
92
Use Overriding Operand Size
No
94
Operand Size = 32 Bits
End

Fig. 5

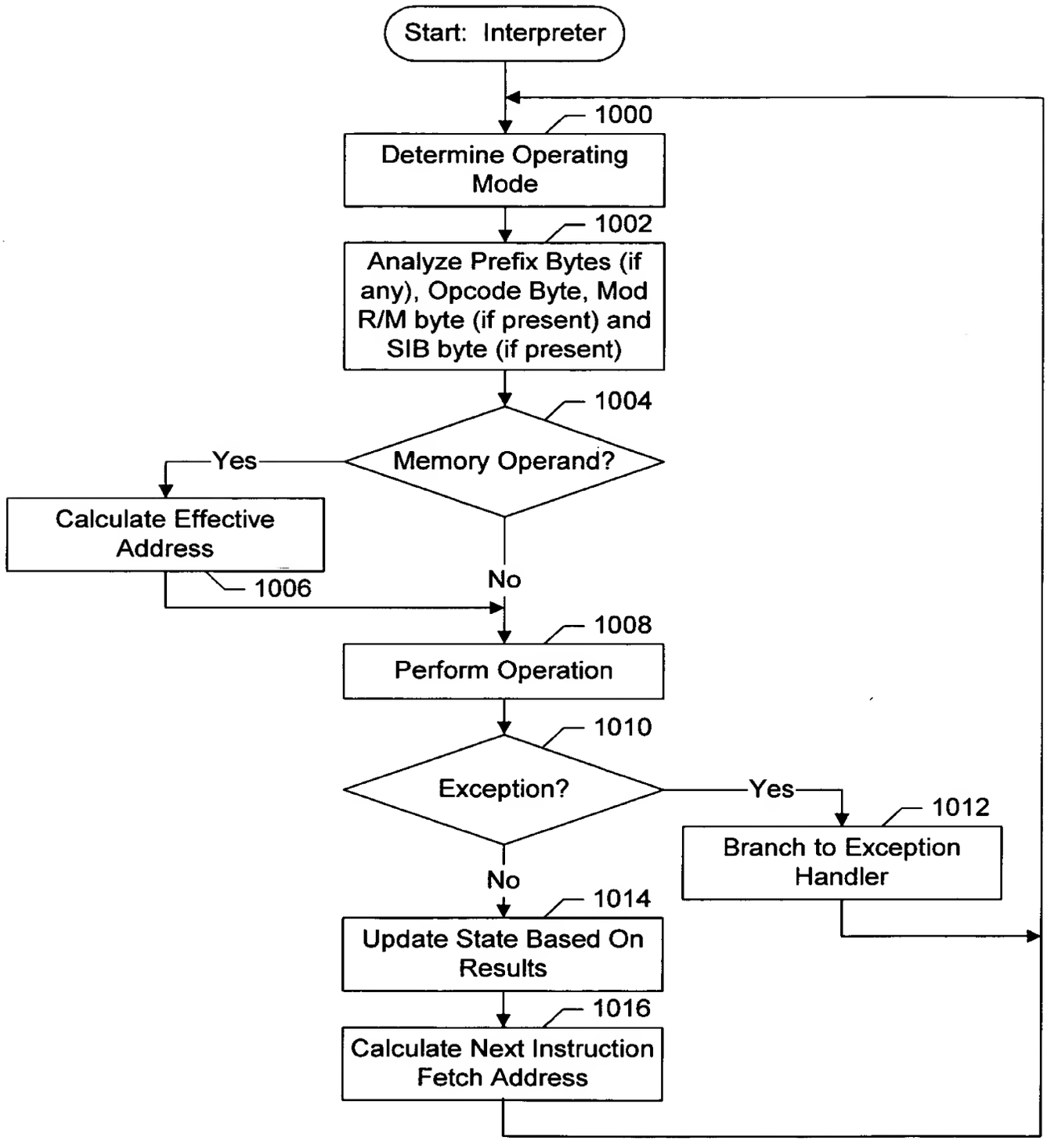
Start: Interpreter
1000
Determine Operating Mode
1002
Analyze Prefix Bytes (if any), Opcode Byte, Mod R/M byte (if present) and SIB byte (if present)
1004
Memory Operand?
Yes
Calculate Effective Address
1006
No
1008
Perform Operation
1010
Exception?
Yes
1012
Branch to Exception Handler
No
1014
Update State Based On Results
1016
Calculate Next Instruction Fetch Address

Fig. 6

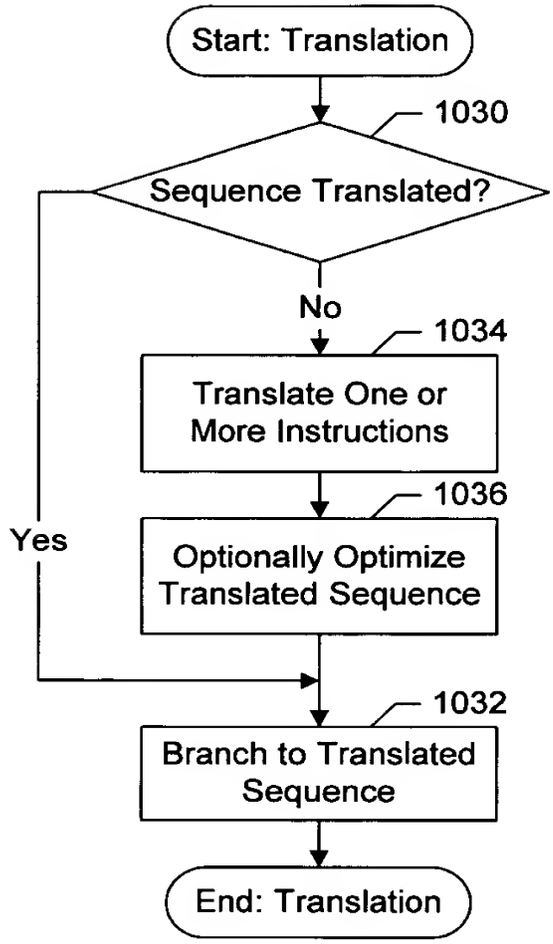
Start: Translation
1030
Sequence Translated?
No
1034
Translate One or More Instructions
1036
Optionally Optimize Translated Sequence
Yes
1032
Branch to Translated Sequence
End: Translation

Fig. 7

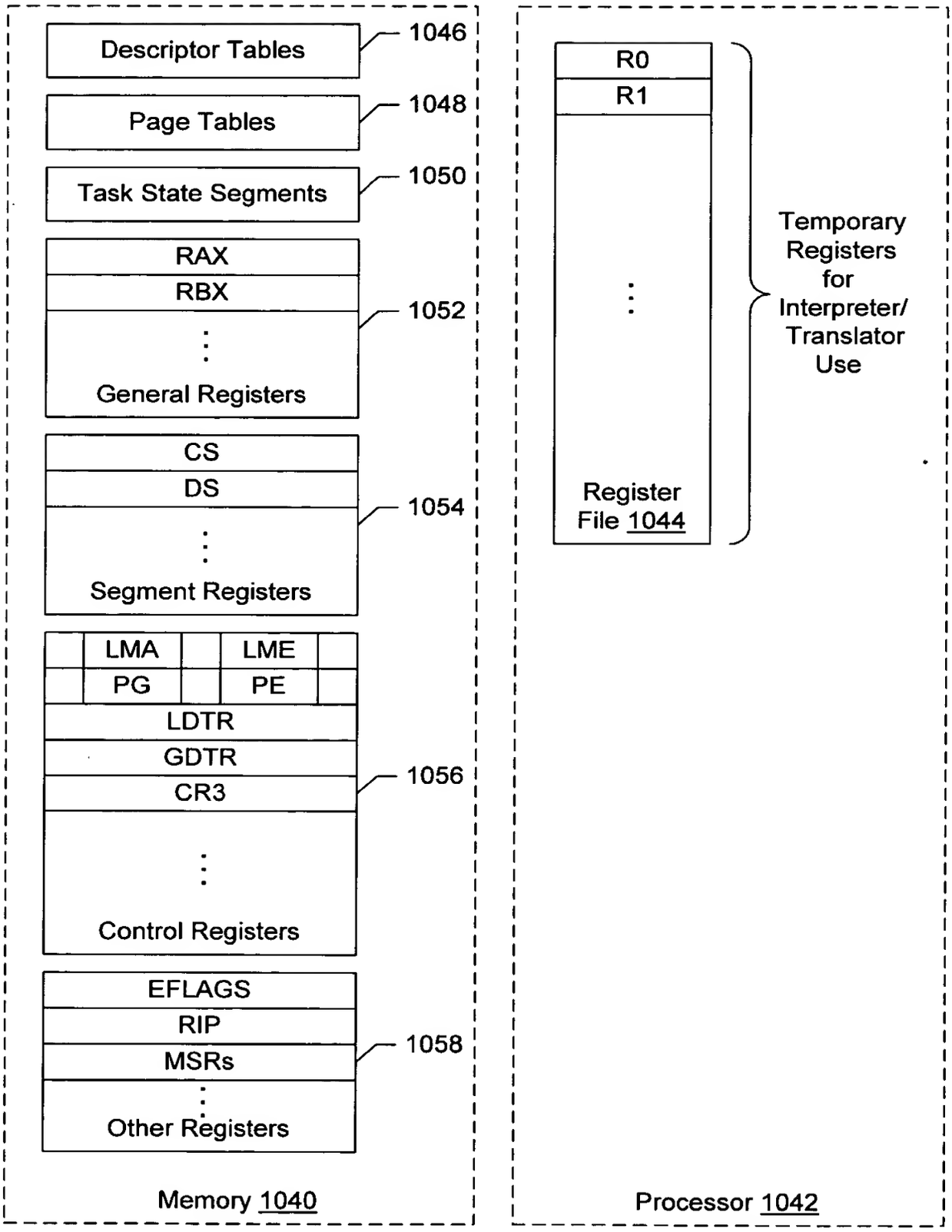
Descriptor Tables
1046
Page Tables
1048
Task State Segments
1050
RAX
RBX
General Registers
1052
CS
DS
Segment Registers
1054
LMA
LME
PG
PE
LDTR
GDTR
CR3
Control Registers
1056
EFLAGS
RIP
MSRs
Other Registers
1058
Memory 1040
R0
R1
Register File 1044
Temporary Registers for Interpreter/ Translator Use
Processor 1042

Fig. 8

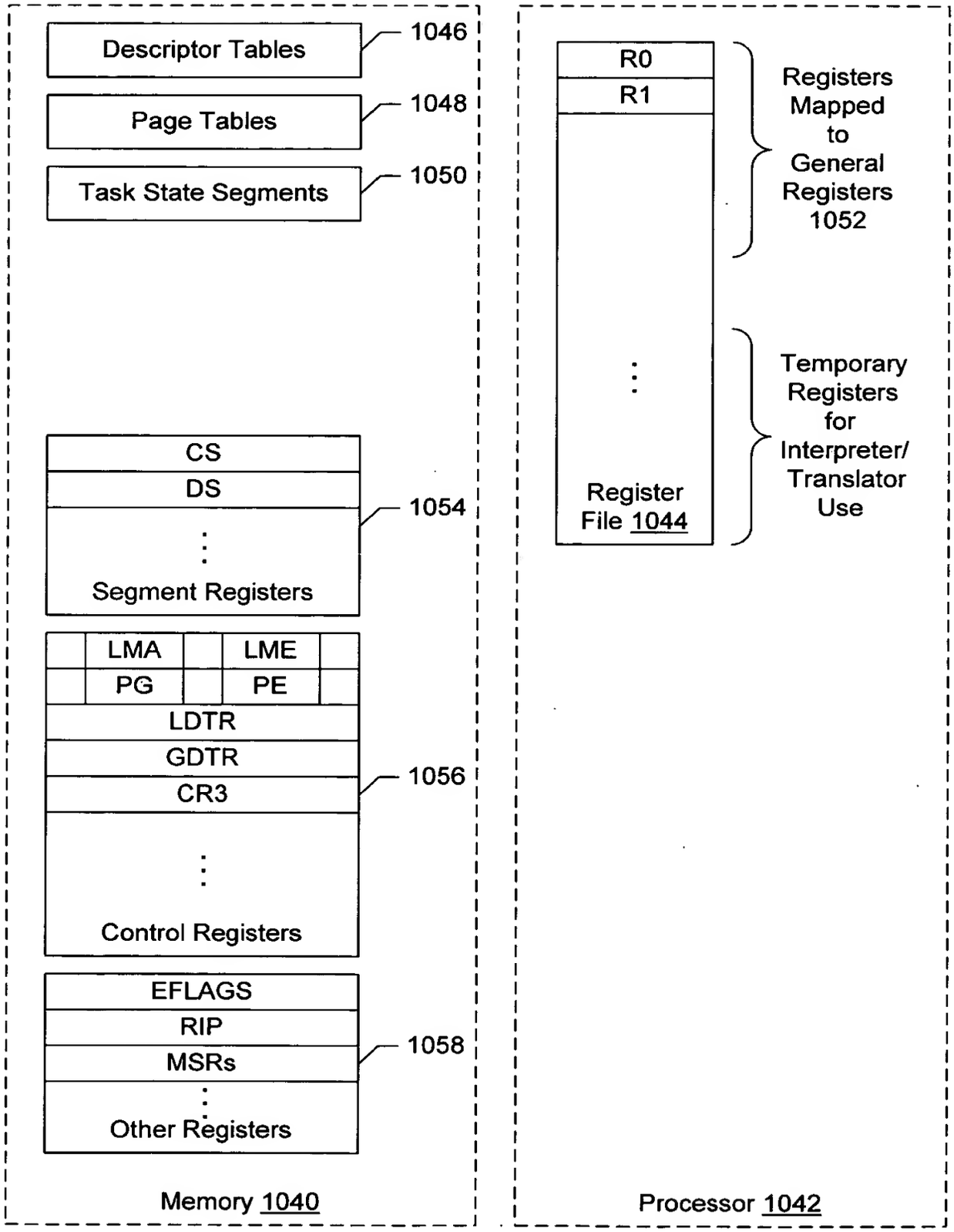
Descriptor Tables
1046
Page Tables
1048
Task State Segments
1050
CS
DS
Segment Registers
1054
LMA
LME
PG
PE
LDTR
GDTR
CR3
Control Registers
1056
EFLAGS
RIP
MSRs
Other Registers
1058
Memory 1040
R0
R1
Register File 1044
Registers Mapped to General Registers 1052
Temporary Registers for Interpreter/ Translator Use
Processor 1042

Fig. 9

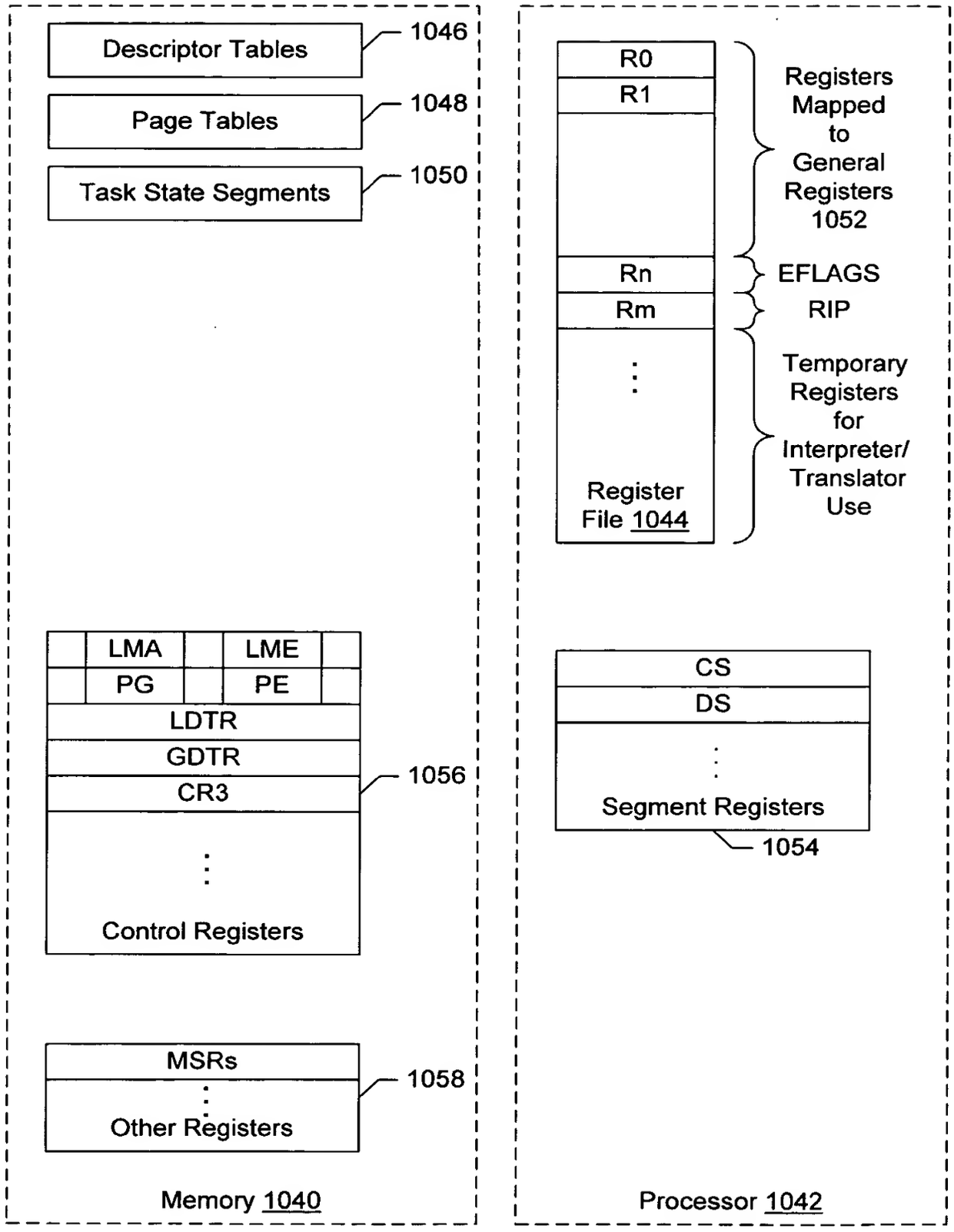
Descriptor Tables
1046
Page Tables
1048
Task State Segments
1050
LMA
LME
PG
PE
LDTR
GDTR
CR3
Control Registers
1056
MSRs
Other Registers
1058
Memory 1040
R0
R1
Rn
Rm
Register File 1044
Registers Mapped to General Registers 1052
EFLAGS
RIP
Temporary Registers for Interpreter/ Translator Use
CS
DS
Segment Registers
1054
Processor 1042

Fig. 10

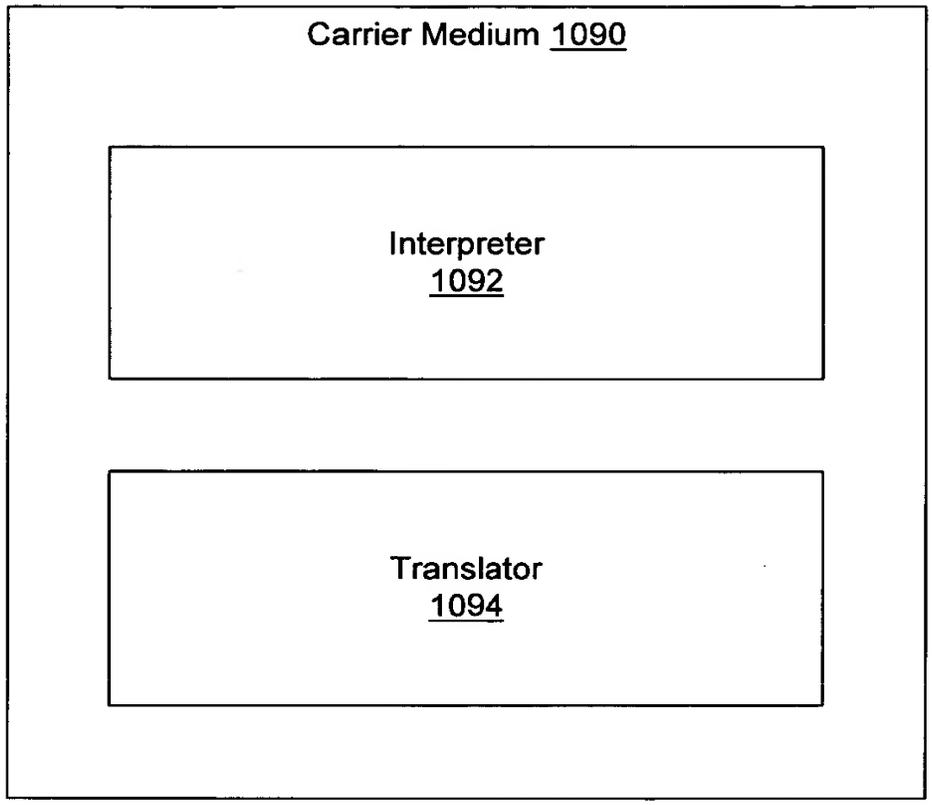

Fig. 11

Docket No. 50277-0810

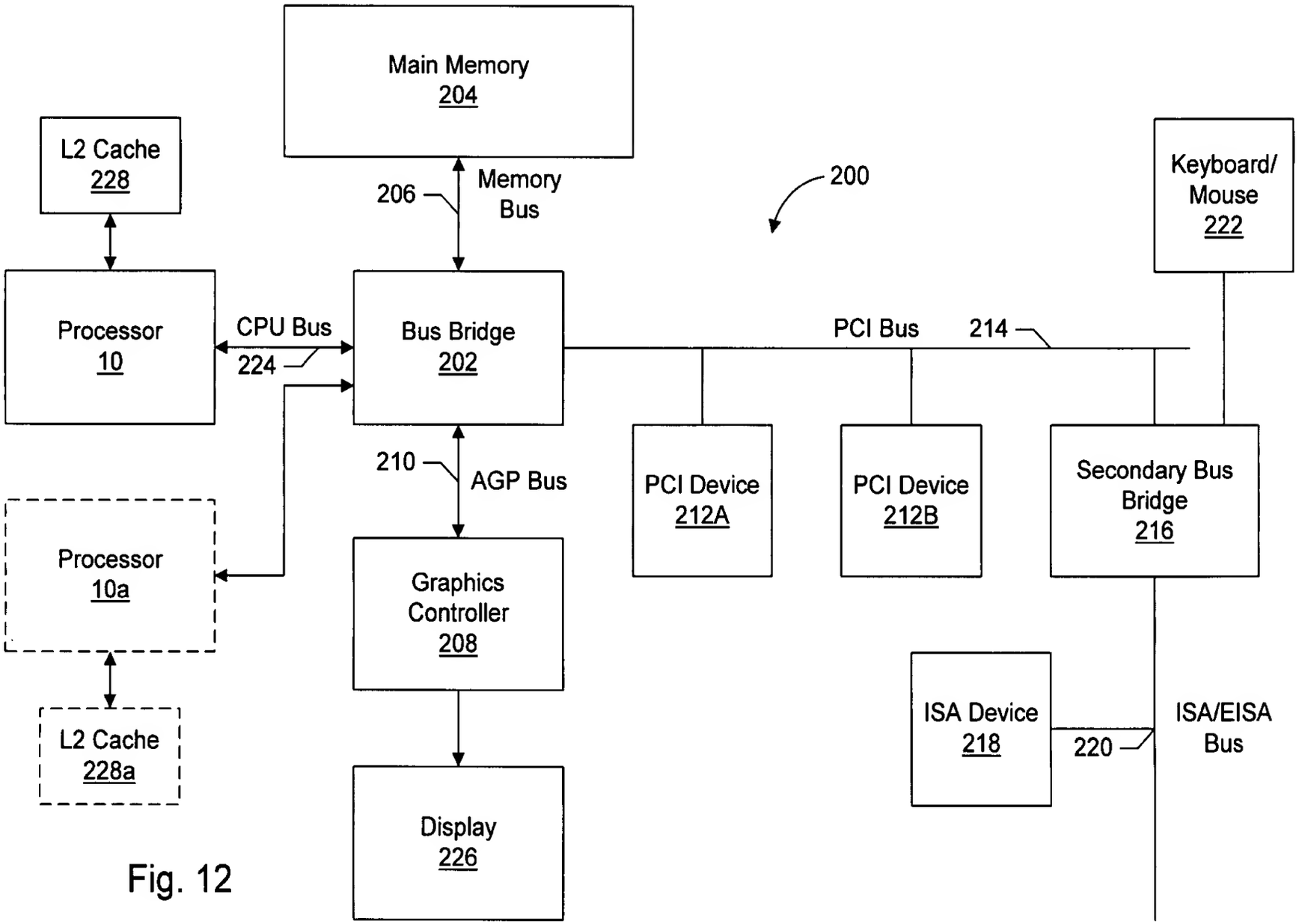
Main Memory
204
L2 Cache
228
206
Memory
Bus
200
Keyboard/
Mouse
222
Processor
10
CPU Bus
224
Bus Bridge
202
PCI Bus
214
210
AGP Bus
PCI Device
212A
PCI Device
212B
Secondary Bus
Bridge
216
Processor
10a
Graphics
Controller
208
ISA Device
218
220
ISA/EISA
Bus
L2 Cache
228a
Display
226

Fig. 12

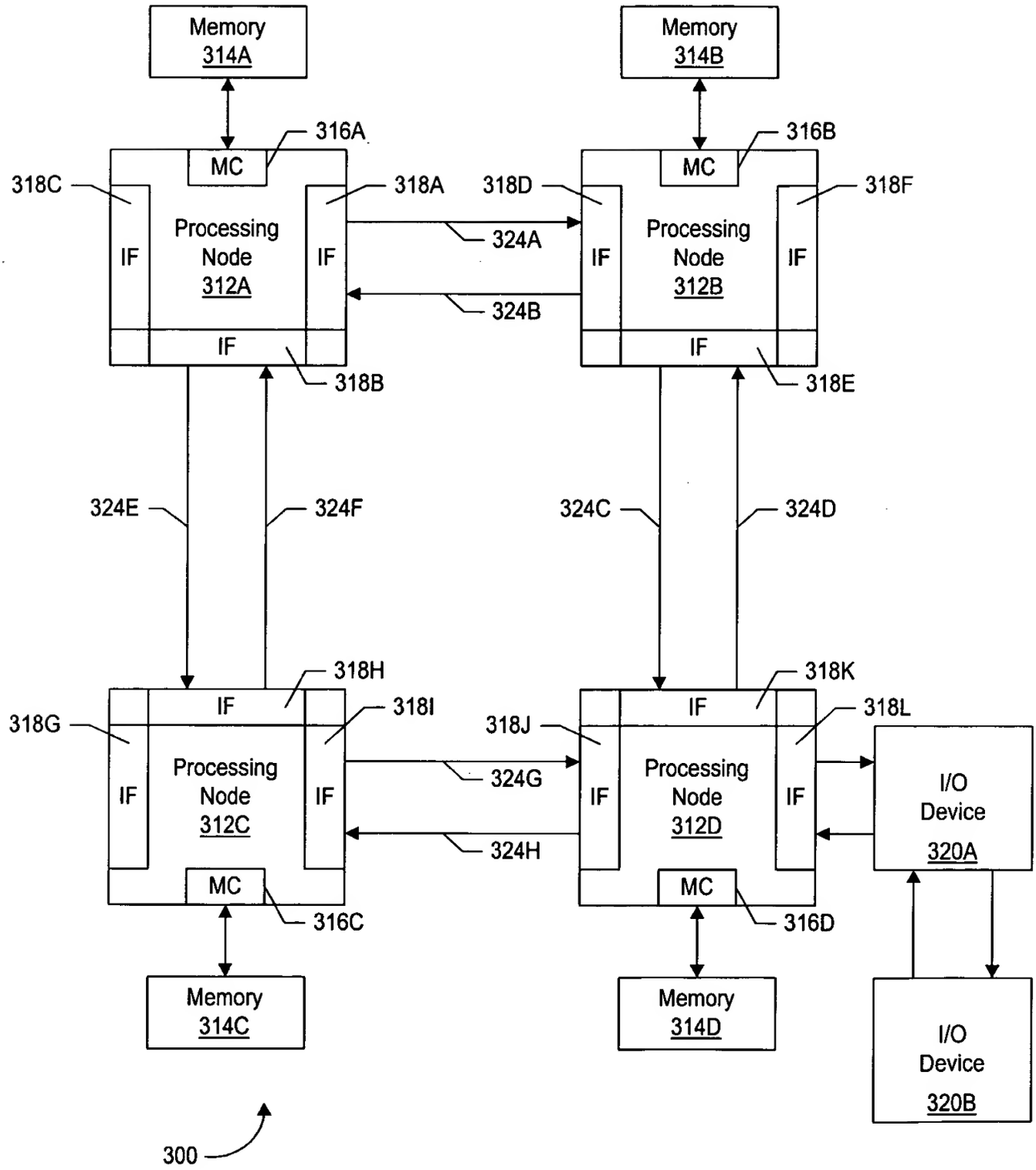
Memory
314A
Memory
314B
316A
316B
MC
MC
318C
318A
318D
318F
IF
Processing
Node
312A
IF
IF
Processing
Node
312B
IF
324A
324B
IF
IF
318B
318E
324E
324F
324C
324D
318H
318K
IF
IF
318G
318I
318J
318L
IF
Processing
Node
312C
IF
IF
Processing
Node
312D
IF
I/O
Device
320A
324G
324H
MC
MC
316C
316D
Memory
314C
Memory
314D
I/O
Device
320B
300

Fig. 13